



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Cobbley et al.

Serial No.: 10/693,286

Filed: October 23, 2003

For: METHOD FOR MANUFACTURING
FLIP-CHIP SEMICONDUCTOR
ASSEMBLY

Confirmation No.: 2348

Examiner: T. Nguyen

Group Art Unit: 2813

Attorney Docket No.: 2269-3437.7US
(97-0514.07/US)

Notice of Allowance Mailed:

January 11, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994823379US

Date of Deposit with USPS: April 8, 2005

Person making Deposit: Steve Wong

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of \$1,715.00 in payment therefor plus five (5) copies of the patent when issued.

Also enclosed are Amendment Pursuant to 37 C.F.R. § 1.312(a); Comments on Statement of Reasons for Allowance; and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees.

Applicants understand that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,



Kevin K. Johanson
Registration No. 38,506
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: April 8, 2005

KKJ/dlm:sg

Enclosures: Part B - Issue Fee Transmittal

Check No. 21543 in the amount of \$1,715.00

Copy of Transmittal Letter

Amendment Pursuant to 37 C.F.R. § 1.312(a) (5 pages)

Comments on Statement of Reasons for Allowance (2 pages)

Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages)

Document in ProLaw



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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner indicates:

[None of the references of record teaches or suggests the claimed method for in situ electrical testing of a flip-chip assembly during its manufacturing including while the substrate is in contact with the plurality of probes and the one or more IC dice are positioned on the surface of the substrate, and before sealing of the one or more IC dice, electrically testing the flip-chip semiconductor assembly using the plurality of probes; repairing the flip-chip semiconductor assembly if it fails the electrical testing, or bringing one or more IC dice into a flip-chip type conductive contact with the substrate while it is connected to the test apparatus at

the die-attaching station to form the flip-chip semiconductor assembly; and electrically testing the assembly.]

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'K. Johanson', with a long horizontal flourish extending to the right.

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Date: April 8, 2005
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